CLAIMS

What is claimed is:

1. A radio frequency (RF) to baseband interface providing power control over an RF section that processes RF signals and that is coupled to a baseband section that processes baseband signals, the interface comprising:

a bi-directional message interface for communicating a power control message from the baseband section to the RF section; and

a data interface for communicating data from the RF section to the baseband section.

2. The interface of claim 1, where the power control message comprises a power control bit specifying a power state for pre-selected circuitry in the RF section.

3. The interface of claim 2, where the power state is one of a power-up state and a power-down state.

4. The interface of claim 1, where the power control message comprises a plurality of power control bits individually specifying power states for a plurality of pre-selected circuitry in the RF section.

5. The interface of claim 2, where the pre-selected circuitry is at least one of a frequency divider, oscillator, and amplifier.

6. The interface of claim 1, where the message interface is a serial message interface.

7. The interface of claim 1, where the message interface comprises a message-in signal line, a message-out signal line and a message clock signal line.

8. A method for controlling power in a radio frequency (RF) section that processes RF signals and that is coupled to a baseband section that processes baseband signals, the method comprising the steps of:

setting a power control bit in a power control message; and

communicating the power control message over a message interface from the baseband section to the RF section.

9. The method of claim 8, wherein the step of communicating comprises the step of serially communicating the power control message.

10. The method of claim 8, wherein the step of communicating comprises the step of serially communicating the power control message using a message-in signal line, a message-out signal line and a message clock signal line.

11. The method of claim 8, where the power control bit specifies a power state for pre-selected circuitry in the RF section.

12. The method of claim 11, where the power state is one of a power-up state and a power-down state.

13. The method of claim 8, where the step of setting comprises the step of setting a plurality of power control bits individually specifying power states for a plurality of pre-selected circuitry in the RF section.

14. An RF front end for a satellite positioning system receiver, the front end comprising:

an RF processing section comprising an RF input for receiving satellite positioning system signals; and

an RF to baseband interface coupled to the RF processing section, the interface comprising:

a bi-directional message interface for communicating messages between the RF processing section and a baseband processing section, including receiving a power control message from the baseband processing section; and

a data interface for communicating data from the RF processing section to the baseband processing section.

15. The RF front end of claim 14, wherein the message interface comprises:

a message clock line;

a message-in signal line and

a message-out signal line; and

wherein the message-out signal line carries an output bit stream representing the power control message.

16. The RF front end of claim 15, where the power control message comprises a power control bit specifying a power state for pre-selected circuitry in the RF section.

17. The RF front end of claim 16, where the power state is one of a power-up state and a power-down state.

18. The RF front end of claim 15, where the power control message comprises a plurality of power control bits individually specifying power states for a plurality of pre-selected circuitry in the RF section.

19. The RF front end of claim 15, where the pre-selected circuitry is at least one of a frequency divider, oscillator, and amplifier.

20. The RF front end of claim 15, where the data interface comprises a data clock signal line and a data bit signal line.

21. The RF front end of claim 20, where:

the data clock signal line carries a data clock comprising a rising edge and a falling edge;

the data bit signal line carries a data signal comprising a sign bit and a magnitude bit; and

the first data bit is valid on the rising edge of the data clock and the second data bit is valid on the falling edge of the data clock.

22. A baseband back end for a satellite positioning system receiver, the back end comprising:

a baseband processing section comprising at least one address, data, and control line for communicating with a digital device; and

an RF to baseband interface coupled to the baseband processing section, the interface comprising:

a bi-directional message interface for communicating messages between an RF processing section and the baseband processing section, including communicating a power control message to the RF processing section; and

a data serial interface for communicating data from the RF processing section to the baseband processing section.

23. The baseband back end of claim 22, wherein the message serial interface comprises:

a message clock line;

a message-in signal line and

a message-out signal line; and

wherein the message-out signal line carries an output bit stream representing the power control message.

24. The baseband back end of claim 22, where the power control message comprises a power control bit specifying a power state for pre-selected circuitry in the RF processing section.

25. The baseband back end of claim 24, where the power state is one of a power-up state and a power-down state.

26. The baseband back end of claim 22, where the power control message comprises a plurality of power control bits individually specifying power states for a plurality of pre-selected circuitry in the RF section.

27. The baseband back end of claim 26, where the pre-selected circuitry is at least one of a frequency divider, oscillator, and amplifier.

28. A satellite positioning system receiver comprising:

an RF front end comprising an RF processing section and an RF input for receiving satellite positioning system signals;

a baseband back end comprising a baseband processing section and at least one address, data, and control line for communicating with a digital device; and

an RF to baseband interface coupled between the RF processing section and the baseband processing section, the interface comprising:

a bi-directional message interface for communicating messages between the RF processing section and the baseband processing section, including communicating a power control message to the RF processing section; and

a data interface for communicating data from the RF processing section to the baseband processing section.

29. The satellite positioning system receiver of claim 28, wherein the message interface comprises:

a message clock line;

a message-in signal line and

a message-out signal line; and

wherein the message-out signal line carries an output bit stream representing the power control message.

30. The satellite positioning system receiver of claim 29, where the power control message comprises a power control bit specifying a power state for pre-selected circuitry in the RF processing section.

31. The satellite positioning system receiver of claim 30, where the power state is one of a power-up state and a power-down state.

32. The satellite positioning system receiver of claim 29, where the power control message comprises a plurality of power control bits individually specifying power states for a plurality of pre-selected circuitry in the RF section.

33. The satellite positioning system receiver of claim 32, where the pre-selected circuitry is at least one of a frequency divider, oscillator, and amplifier.